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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,745	08/01/2003	Hui Xu	10030329-1	3868

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EXAMINER	
LE, LANA N	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 11/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,745	XU ET AL.	
	Examiner	Art Unit	
	Lana N. Le	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 9/21/06

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) 20 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-2, 5, 8-9, 13, and 18-20 are rejected under 35 U.S.C. 103(a) as being anticipated by Bosnyak et al (US 6,515,501).

Regarding claim 1, Bosnyak et al disclose a communications module (fig. 3), comprising:

a data channel (data path 108 stored within signal buffer (SB) 304 for retransmission) operable to translate data signals (reconstitute a signal; col 7, lines 25-30) in at least one direction between a transmission line interface (signal buffer 302) (col

4, lines 4-6) and a host device interface (interface between SB 304 and IC 104) (col 7, lines 18-39; col 6, line 59 – col 7, line 4), and having a variably configurable termination impedance at a host device node (node at connection line between 304 and 104) connectable to a host device (104) (col 3, line 66 – col 4, line 4) (col 4, lines 52-60); and

a termination impedance controller (impedance control circuit 508, 510; fig. 5) operable to set the variably configurable termination impedance (Zin, Zout) of the data channel (data paths within 304) (col 4, line 66 – col 5, line 24).

Regarding claim 2, Bosnyak et al disclose the communications module of claim 1, wherein the data channel comprises a variable resistance circuit (matched variable Zout controlled by 510 to Sout of buffer; fig. 5) at the host device node (node 504 at connection line between 304 and 104) (col 5, lines 12-15).

Regarding claim 5, Bosnyak et al disclose the communications module of claim 2, wherein the variable resistance circuit presents different termination impedances (Zin, Zout) at the host device node (node at connection line between 304 and 104) in response to receipt of different respective electrical control signals from the termination impedance controller (508, 510) (col 4, line 66 – col 5, line 24).

Regarding claim 8, Bosnyak et al disclose the communications module of claim 1, further comprising a housing (304) containing the data channel (data path 108).

Regarding claim 9, Bosnyak et al disclose the communications module of claim 8, wherein the housing (304) has a transmission cable interface end (terminating impedance of transmission line interfaced within buffer 304 to match with Zin of data channel stored in 304) and a host device interface end (input impedance of IC device

interfaced within buffer 304 to match with Zout of data channel stored in 304) (fig. 3).

Regarding claim 13, Bosnyak et al disclose the communications module of claim 1, wherein the data channel (108, 304) provides multiple channel transmission of data (multiple data transmission 108) in at least one direction (direction toward the right) between the transmission cable interface (interface from SB 302 to SB 304) and the host device interface (interface from SB 304 to IC 104).

Regarding claim 18, Bosnyak et al disclose a method of making a communications module, comprising:

obtaining a data channel (data signal path 108) operable to translate data signals (reconstitute data signals) in at least one direction (direction to the right) between a transmission cable interface (buffer interface 302) and a host device interface (interface between 304 and IC 104) (col 7, lines 18-39) and having a variably configurable termination impedance at a host device node (504) connectable to a host device (104) (col 6, line 59 – col 7, line 4);

mounting the data channel (108) in a housing (304) having a first end connectable to a transmission cable (transmission line 108) and a second end connectable to a host device (104) (col 7, lines 18-39); and

setting the variably configurable termination impedance of the data channel to a termination impedance value (Zout) substantially matching a target host device (IC 104) termination impedance value (col 4, lines 52-57; col 4, line 66 – col 5, line 24).

Regarding claim 19, Bosnyak et al disclose the method of claim 18, wherein the variably configurable termination impedance of the data channel is set (via 510) after

the data channel is mounted in the housing (304) (col 4, line 52 – col 5, line 24).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bosnyak et al (6,515,501) in view of Jean et al (US 6,407,639).

Regarding claim 3, Bosnyak et al disclose the communications module of claim 2, wherein Bosnyak et al do not disclose the variable resistance circuit comprises a transistor with a voltage-controlled resistance value. Jean et al disclose a variable resistance circuit comprises a transistor (T) with a voltage-controlled resistance value (resistance of T is controlled by voltage via node 15) (col 3, lines 20-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the variable resistance circuit have a transistor with a voltage-controlled resistance value in order to stabilize the output to the output device as suggested by Jean et al.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bosnyak et al (6,515,501) in view of Bogli (US 6,385,547).

Regarding claim 4, Bosnyak et al disclose the communications module of claim 2, wherein Bosnyak et al do not disclose the variable resistance circuit comprises a resistor connected in series with a switch. Bogli discloses a variable resistance circuit (28) comprises a resistor (43) connected in series with a switch (37) (col 2, lines 39-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a variable resistor connected with a switch in order to impose a resistance only when needed via closing the switch to avoid overloading of high voltage as suggested by Bogli.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bosnyak et al (6,515,501).

Regarding claim 7, Bosnyak et al disclose the communications module of claim 1, wherein the termination impedance controller (508, 510) is operable to selectively set the variably configurable termination impedance of the data channel to a differential resistance in a first configuration mode and to set the variably configurable termination impedance of the data channel to a desired differential resistance in a second configuration mode (col 5, line 36 - col 6, line 16). Bosnyak et al do not specifically disclose a resistance value of 100 and 150 ohms. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the impedances to a specific complex resistance value in order to achieve a desired impedance.

7. Claims 10-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bosnyak et al (6,515,501) in view of Flickinger et al (US 6,418,121).

Regarding claim 10, Bosnyak et al disclose the communications module of claim 9, wherein Bosnyak et al do not disclose the host device interface end of the housing is pluggable into a receptacle of a host device. Flickinger et al disclose the host device interface end of the housing (module plug) is pluggable into a receptacle of a host device (terminating end of guide structure mounted to host; col 1, lines 35-65; col 2, lines 13-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to plug the interface end of the housing into a receptable of a host device in order to supply power to the module from the host.

Regarding claim 11, Bosnyak et al disclose the communications module of claim 1 wherein Bosnyak et al do not disclose implemented in accordance with a small form pluggable (SFP) configuration or a small form factor (SFF) configuration. Flickinger et al disclose a module implemented in accordance with a small form factor (SFF) configuration (col 2, lines 10-24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a small form factor in the IC containing the transceiver module of Bosnyak et al to give gigabaud data capability for fibre channel and transmission media as suggested by Flickinger et al (col 1, lines 20-34).

Regarding claim 12, Bosnyak et al disclose the communications module of claim 1 wherein Bosnyak et al do not disclose the module is implemented in accordance with a Giga-Bit Interface Converter (GBIC) configuration. Flickinger et al disclose a module implemented in accordance with a Giga-Bit Interface Converter (GBIC) configuration (col 2, lines 10-24; col 1, lines 20-34). It would have been obvious to one of ordinary

skill in the art at the time the invention was made to implement the module in a GBIC provide a single small form factor to give gigabaud data rate capability for fibre channel and transmission media as suggested by Flickinger et al (col 1, lines 20-34).

Regarding claim 14, Bosnyak et al disclose the communications module of claim 1, wherein Bosnyak et al do not disclose the data channel is operable to translate data signals in both directions between the transmission cable interface and the host device interface. Flickinger et al disclose the data channel is operable to translate data signals in both directions between the transmission cable interface and the host device interface (col 1, lines 39-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to translate data in both directions in order to allow the host device to communicate and drive the communication module as suggested by Flickinger et al.

8. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bosnyak et al (6,515,501) in view of Flickinger et al (US 6,418,121) and further in view of Drost et al (US 6,738,415).

Regarding claim 15, Bosnyak et al disclose a communications module (fig. 3), comprising:

a receiver data channel (data path 108 stored within signal buffer (SB) 304 for retransmission) operable to translate data signals (reconstitute data signals; col 7, lines 25-30) from a transmission cable interface (signal buffer 302) (col 4, lines 4-6) to a host device interface (interface from SB 304 to IC 104) (col 7, lines 18-39; col 6, line 59 – col 7, line 4) (col 7, lines 18-39), wherein each of the receiver data channel (data signal

path 108) has a respective variably configurable termination impedance (variable Zin, Zout controlled by 508, 510) at a respective host device node (node at connection line between 304 and 104) connectable to the host device (104) (col 3, line 66 – col 4, line 4; col 4, lines 52-60); and

a termination impedance controller (508, 510; fig. 5) operable to set the respective variably configurable termination impedance (variable Zin, Zout) of each of the receiver data channel (data signal path 108); and

a housing (304) containing the receiver data channel (108) and the termination impedance controller (508, 510), and having a transmission cable interface end (504 of SB 302; fig. 5) connectable to a transmission cable (to transmission line 108) and a host device interface end (interface between 304 and IC 104) connectable to a host device (104) (col 3, line 66 – col 4, line 4, col 4, lines 52-60).

Bosnyak et al do not disclose a transmitter data channel operable to translate data signals from the host device interface to the transmission cable interface, the housing containing a transmitter data channel. Flickinger et al disclose a transmitter data channel (transmission data signal path) operable to translate data signals from the host device interface (transmission conversion circuit within gigabit interface converter module (GBIC) is inserted in a host) to the transmission cable interface (wire transmission medium); a housing containing the transmitter data channel (GBIC module containing transmission data signals received from host device) (col 1, lines 32-38, lines 53-65; col 2, lines 13-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a transmitter data channel in order to

transmit data signals from the host interface to the transmission cable interface of Bosnyak et al in order to allow the host device interface to provide amplified differential signals to the transmission line interface as suggested by Flickinger et al.

Bosnyak and Flickinger et al do not disclose each of the receiver data channel and the transmitter data channel has a respective variably configurable termination impedance at a respective host device node connectable to the host device. Drost et al disclose each of transmitter data channel (bidirectional data channel) has a respective variably configurable termination impedance at a respective host device node (node connecting the device 508) connectable to the host device (IC 504) and an inherent termination impedance controller to select the impedance for the transmitter data channel (col 6, lines 43-48; fig. 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have variable impedances in order to allow the data signals sent from the host device for feedback to the transmission cable to be selected at the connection node to the host device as suggested by Drost et al.

Regarding claim 16, Bosnyak et al, Flickinger et al, and Drost et al disclose the communications module of claim 15, wherein Bosnyak et al disclose each of the receiver data channel comprises a respective variable resistance circuit (matched Zout to Zout of host interface 304) at the respective host device node (Sout 504; fig. 5) (col 5, lines 12-15), and Drost et al further disclose the transmitter data channel comprises a respective variable resistance circuit (selective impedance from data signals 506) at the respective host device node (node at 508).

Regarding claim 17, Bosnyak et al, Flickinger et al, and Drost et al disclose the

communications module of claim 16, wherein Bosnyak et al disclose each variable resistance circuit presents different termination impedances (Zout) at the respective host device node (504) in response to receipt of different respective electrical control signals from the termination impedance controller (508, 510) (col 4, line 66 - col 5, line 24).

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bosnyak et al (6,515,501) in view of Migayawa et al (5,553,250).

Regarding claim 6, Bosnyak et al disclose the communications module of claim 2, wherein Bosnyak et al do not disclose the variable resistance circuit comprises a mechanical switch for selectively connecting the host device node to different termination impedances (col 1, line 64 – col 2, line 30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to match impedances so that the binary signal can be transmitted as an accurate square wave on the bus line between the initiator and the target as suggested by Migayawa et al. Bosnyak et al and Migayawa et al do not disclose the termination impedance controller enables manual control of the mechanical switch. However, it is well known and notoriously old in the art to manually actuate a mechanical switch. It would have been obvious to one of ordinary skill in the art at the time the invention was made to manually control the mechanical switch in order to allow the user to control the switch to a desired impedance function.

Response to Arguments

10. Applicant's arguments filed 9/21/06 have been fully considered but they are not persuasive. Regarding claims 1 and 15, applicant argues the signal buffer 302 does not connect to any cable and the reference cited, Bosnyak does not have a transmission cable interface. The examiner respectfully disagrees. The signal trace 108 is a transmission line (see col 2, lines 6-12) wherein a transmission line is defined to be old and well known in the art as a coaxial cable (see Newton's Telecom Dictionary). The signal buffer temporarily stores and hold the signals for retransmission and serves as a shared boundary to convey information to the SB 304 and therefore, acts as a cable interface between the transmission cable and the host device interface.

Regarding claim 18, applicant argues the reference cited signal buffer is mounted in a housing having a first end connectable to a transmission cable. The examiner respectfully disagrees. However, the buffer itself is a housing to store the transmitted signal going through the transmission cable 108 and the first end is connectable to signal cable 108 connected from block 302.

Regarding claim 10, the secondary reference is cited to show that an interface module is pluggable into the host device which is obvious to one of ordinary skill in the art since the host interface end must somehow be connected to the host via the transmission cable 108.

Allowable Subject Matter

11. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 20, Bosnyak et al disclose the method of claim 18, wherein the cited prior art fail to disclose further comprising storing the communication module before the variably configurable termination impedance of the data channel is set.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N. Le whose telephone number is (571) 272-7891. The examiner can normally be reached on M-F 9:30-18:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lana Le

Lana N. Le
11-26-06
LANA LE
PRIMARY EXAMINER